Abstract of the Disclosure

A processor is provided that is a programmable digital signal processor (DSP) with variable instruction length, offering both high code density and easy programming. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms, such as for wireless telephones, as well as pure control tasks. A coefficient data pointer is provided for accessing coefficient data for use in a multiply-accumulate (MAC) unit. Monitoring circuitry determines when the coefficient data pointer is modified (step 1104). When an instruction is executed (step 1102) that requires a coefficient datum from memory in accordance with the coefficient data pointer, a memory access is inhibited (step 1108) if the coefficient data pointer has not been modified since the last time a memory fetch was made in accordance with the coefficient data pointer and the previously fetched coefficient datum is reused. However, if the coefficient data pointer was modified since the last time a memory fetch was made in accordance with the coefficient data pointer, then the required coefficient datum is fetched from memory (step 1106). A shadow register within the MAC unit execution pipeline temporarily saves coefficient data for possible reuse.